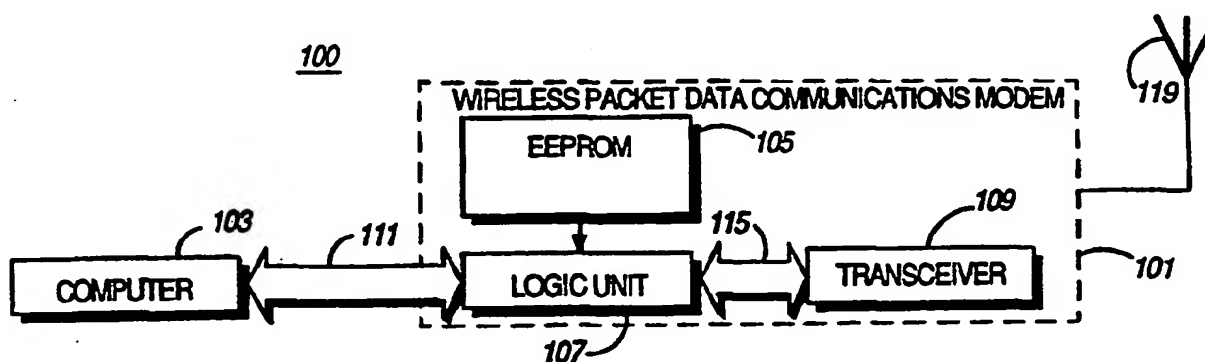


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(54) Title: A WIRELESS PACKET DATA COMMUNICATIONS MODEM AND METHOD OF USE THEREIN



(57) Abstract

A computing device (100) including a wireless packet data communications modem (101) used in conjunction with a computer (103) to provide untethered access to data bases and other computer users. A method is provided for controlling data transmission and reception using the wireless packet data communications modem (101) in tandem with the computer (103). Two-way communications is achieved using a small, low-cost, light-weight wireless packet data communications modem contained in a housing, integral to a computing device, or a removable housing conforming to a PCMCIA industry standard.

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A Wireless Packet Data Communications Modem
And Method Of Use Therein

This is a continuation-in-part of application Serial No. 08/143,689,
filed on October 28, 1993.

Field Of The Invention

This disclosure deals generally with wireless
communications modems and more specifically but not limited to
packet data communications modems cooperatively arranged with
computing devices.

Background Of The Invention

As the information age continues to unfold the utility
associated with, if not necessity of, untethered communications
has become increasingly apparent. That such communications
should include data may be self evident. The local translation and
manipulation of local or remote data, requisite to the production
of information, virtually mandates a degree of associated local
computing capability. Practitioners, attempting to serve this
untethered or portable marketplace, have labored to provide
products with varying degrees of the requisite utility.

Portable wireless data terminals allowing the transmission
to remote locations of local data as well as the reception and
display of remote data are now known. These data terminals lack
the storage and operator interface capabilities and flexibility
ordinarily associated with a plausible computing device. Likewise
portable computers have been shown. Such computers having
wireline access to remote databases by way of the public switched
telecommunications network are available. Portable computers
with the capability of wireless reception of data have been
demonstrated. These computers all lack the highly coveted
attribute of two way wireless access to remote data bases. Similarly,

rudimentary wireless data transceivers arranged to be utilized with portable computers, although contemplated, lack even the elementary intelligence or processing capability required for media access.

5 In all of these endeavors to satisfy this untethered and portable marketplace, practitioners have been limited by the realities of technology and human imagination. Products must simultaneously be useful and convenient to the individual on the move. Today this implies extensive communications and
10 computing capabilities together with sufficient battery life all in a physical size and weight that is practical for an individual on the move. That one or more requisite attributes is lacking in all of the known and contemplated products has been shown. Neither is a mere combination of such products an answer given the practical
15 constraints on size, weight, and battery life either in combination or singularly. Clearly an urgent need exists for a wireless packet data communications modem that addresses the attributes required by the untethered marketplace.

20

Brief Description Of The Drawings

The features of the present invention which are believed to be novel are set forth with particularity in the appended claims.
25 However, the invention together with further advantages thereof, may best be understood by reference to the accompanying drawings in which:

FIG. 1 is a block diagram of a computing device in accordance with one embodiment of the instant invention.

30 FIG. 2 is a perspective view of a data modem in accordance with one embodiment of the instant invention.

FIG. 3 is a perspective view of a data modem in accordance with an alternative embodiment of the instant invention.

FIG. 4 is a detailed block diagram of a computing device in accordance with a preferred embodiment of the instant invention.

FIG. 4a is a detailed block diagram of a logic unit in accordance with an alternate embodiment of the present invention.

FIG. 5 is a data structure diagram exemplifying one mode of operation of the FIG. 4 embodiment of the instant invention.

FIG. 6 is a data structure diagram exemplifying an alternative mode of operation of the FIG. 4 embodiment of the instant invention.

FIG. 7 is a process flow chart in accordance with a method embodiment of the instant invention.

FIG. 8 is a process flow chart in accordance with an alternative method embodiment of the instant invention.

Detailed Description Of A Preferred Embodiment

Generally the present invention provides an apparatus and method of providing wireless packet data communications in a portable environment where small size, light weight, low power consumption, low cost, and general flexibility are requirements. This is accomplished by an inventive configuration, a wireless packet data communications modem, which operates as a "dumb" peripheral of its host computing device and a method, embodied in a modem driver software routine, which performs packet assembly and disassembly, acknowledgments, message buffering, Automatic Repeat Request (ARQ), and similar network and protocol functions. The modem performs the functions of signal encoding and decoding, error correction, message identification detection, and other hardware support functions.

The wireless packet data communications modem comprises a radio-frequency transceiver and a logic unit, arranged to rely on and operate with an "intelligent" controller, such as a general purpose processor or Digital Signal Processor (DSP) chip,

located external to the packet data communications modem in a preferred embodiment. These processors, along with memories and support circuits, traditionally require a large amount of power to operate, consume a large amount of space, and cost a great deal of money.

5 The packet data modem embodiment of the present invention is typically used integral to a host computing device, and therefore can advantageously eliminate the redundancy of costly power consuming processors by implementing certain signaling and time-critical functions in a custom logic unit and many other logical functions in the host's own processor. The result is a modest additional load on the host processor and a single application specific integrated modem chip based logic unit in place of the expensive, power-hungry, space-wasting multiple processor configuration.

15 The present invention can be more fully described and appreciated with reference to the Figures in which FIG. 1 is a general block diagram of a computing device (100) having wireless packet data communications capability. The computing device (100) includes a wireless packet data communications modem (101) and a computer (103), coupled together at a controller interface (111). In a preferred embodiment, the controller interface (111) is a standard electrical interface, such as the Personal Computer Memory Card International Association (PCMCIA) Card Interface Release 2.0 electrical standard, published by the Personal Computer Memory Card International Association, 1030B East Duane Avenue, Sunnyvale California.

25 The computer (103) is any general-purpose data processor, such as a portable laptop or notebook computer, an electronic organizer, or a desktop computer, including other devices with computer like attributes. The wireless packet data communications modem (101) includes an Electrically Erasable Programmable Read-Only Memory (EEPROM) (105) for storing information required for transmission and reception of data, a

logic unit (107) for performing time critical signaling functions, and a transceiver (109) for sending and receiving radio frequency signals.

5 The transceiver (109) can be configured to operate in conventional technologies, such as Frequency Division Multiple Access (FDMA) or Time Division Multiple Access (TDMA). Also the transceiver (109) could be configured to operate in spread spectrum technologies, such as Code Division Multiple Access (CDMA) or Frequency-Hopped.

10 The controller interface (111) provides power, transmit data blocks, and control information to a logic unit (107) from the computer (103). The controller interface (111) also provides error-corrected, de-interleaved data blocks from the logic unit (107) to the computer (103).

15 The logic unit (107) is electrically connected to the EEPROM (105) and the transceiver (109). The logic unit (107) is used to read various information including, for example, tuning data and message address information from the EEPROM (105). The logic unit (107) also sends a transmit data waveform to the transceiver
20 (109) and receives a de-modulated data signal from the transceiver (109) through an interface (115). The logic unit (107) is generally responsible for various functions including signal encoding and decoding, error correction, message identification detection, and hardware support functions. The Interface (115) includes various
25 control lines, such as transmit or receive switching and frequency programming for the transceiver (109). The transceiver (109) transmits and receives signals through an antenna (119), as is well known in the art.

30 In practice and preferably the data modem (101) will be physically included with the computer (103). This may be facilitated by a physical package that conforms to the PCMCIA industry standard that will be appreciated with reference to FIG. 2 and alternatively to FIG 3.

FIG. 2 shows a perspective view of the primary structural components of one embodiment of the wireless packet data communications modem including an illustrative physical package. The inventive attributes of the present invention, as previously described, facilitate the wireless packet data communications modem's (101) containment in a relatively small housing, approximating the size of the PCMCIA Type II format. The specified dimensions of a PCMCIA Type II package are 85.60 mm X 54.0mm X 5mm.

5 A printed circuit board (PCB) (230) contains or carries electronic devices and one or more integrated circuits or chips that together comprise the wireless packet data communications modem (101). The PCB (230) is sandwiched between a top housing (210) and a bottom housing (240), that are preferably of a material, such as metal or other conductive elements that provides an electro-magnetic interference (EMI) shielding function. The top housing (210), bottom housing (240), and PCB (230) are provided structural support by a chassis (220).

10 The embodiment of the present invention, shown in FIG. 2, is representative of a physical package designed to be largely disposed within a housing of the computer (103). This embodiment shares a power source and a processor with the computer (103), as will be more fully described below.

15 In FIG. 3 a perspective view of another embodiment of the structural components of the present invention is shown. A printed circuit board (PCB) (330) contains electronic devices and integrated circuits, including a processor, that comprise the wireless packet data communications modem (101). The PCB (330) is sandwiched between a top housing (320) and a bottom housing (340), that preferably provide an electro-magnetic interference (EMI) shielding function. The top housing (320), bottom housing (340), and PCB (330) are provided with structural support by a chassis (325).

The chassis (325) also includes a battery housing for a battery (315), which in a preferred embodiment are rechargeable Nickel-Cadmium (NiCad) battery cells. A battery cover (310) encloses the battery housing and the battery (315) as shown. An antenna (305) attaches or is mechanically coupled to the chassis (325) and is electrically connected to the PCB (330) to provide signal reception and transmission capabilities.

The housing depicted in FIG. 3 conforms in part to the PCMCIA Type II standard in that the connector and front card portion of the assembly, defined by the dimensions of the top housing (320), is designed to engage a PCMCIA Type II card slot and connector.

The FIG. 3 embodiment as depicted has its own power source, such as the battery (315) shown, antenna (305), and the processor, as will be more fully described below. The resulting design gives this embodiment some advantages over the FIG. 2 embodiment, including the capability to receive and transmit even if or when physically disassociated from the computer (103). Further this embodiment limits or eliminates any power drain from the host computer (103) and minimizes any computational load, associated with computing tasks during transmission and reception of data, for the computer (103).

For a more thorough description, including the relevant details, of the computing device (100) the reader is referred to FIG. 4 in which like reference numerals refer to like elements from FIG. 1. In FIG. 4, the computing device (100) includes the host computer (103) coupled through the controller interface (111) to the wireless packet data communications modem (101) with the antenna (119).

The computer (103) is comprised of a processor (421), a memory (419), a power source (423), and an operator interface, such as a keyboard and a display (425). These elements are electrically coupled as depicted and well known. The processor (421) writes/reads data to/from the memory (419) via data and

control lines (436). The processor (421) provides an output and accepts an input, respectively, to or from the operator interface (425) via an Input/Output (I/O) bus interface (434). The power source (423) is integral to the computer (103) and provides power to the processor (421), the memory (419), and the operator interface (425).

In one embodiment of the present invention, the housing of the computer (103) contains the wireless packet data communications modem (101). This embodiment shares the power source (423) and the processor (421) with the computer (103). Power is delivered from the power source (423), as opposed to battery (315) in an alternative embodiment, to the controller interface (111) at (440) and from the controller interface (111) to the logic unit (107) at (450). Similarly, data and control information is shared between the processor (421) and the logic unit (107) through the controller interface (111) via a data and a control bus (430, 432).

The logic unit (107) is electrically coupled to the EEPROM (105). Tuning data and message IDs assigned to the computing device 100 are read from the EEPROM into the logic unit (107) and transferred to and from the processor (421) as required and further disclosed in a co-pending application designated PD 05022AV, inventor Beaudoin, et al having a like filing date and assigned to the same assignee as here.

For data transmission, the transceiver (109) is coupled to and controlled by the logic unit (107). The logic unit (107) constructs a data waveform from one or more data blocks sent via the controller interface (111) from the processor (421). The logic unit (107) sends the data waveform to a modulator (417). The modulator (417) modulates a radio-frequency carrier with the data waveform using a synthesizer (404), as is known. The synthesizer (404) is programmed by the logic unit (107) using a control input (405). The control input (405) provides control information including operating parameters for the synthesizer (404).

The modulator (417) performs a type of modulation, such as preferably two or four-level frequency shift keyed modulation (FSK) or a linear type of modulation or other type typically used for wireless data transmission.

5 The modulated waveform is sent to a transmitter (406) for transmission via the antenna (119). Prior to the transmission, a Transmit/Receive (T/R) switch (410) is programmed to a transmit state by the logic unit (107). The logic unit (107) controls the transmitter (406) and the T/R switch (410) via a control path (422).

10 Alternatively, data reception is accomplished utilizing the transceiver (109), which receives a modulated radio frequency carrier via the antenna (119) and a receiver (402), using the synthesizer (404) to provide a receiver reference signal at the appropriate frequency. Prior to the reception the T/R switch (410) must be set to a receive state, as controlled by the logic unit (107).

15 The receiver (402) passes the modulated radio frequency carrier to a demodulator (409), which provides a demodulated data signal to the logic unit (107). The logic unit (107) controls the T/R switch (410), the receiver (402), and the demodulator (409) with control lines (420, 422). This embodiment has the unique advantages of small size, low weight, and low power drain.

20 Alternatively, in another embodiment of the present invention, as shown in FIG. 3, the wireless packet data communications modem (101) can be physically removed from the housing of the computer (103). In this instance, the controller interface (111) is preferably a connector that complies with the PCMCIA interface standard. This embodiment may utilize a separate power source, such as the battery (315) for power and the logic unit (107) may include general processor functionality, as well as the capabilities described above. The processor functionality is similar to that provided by the processor (421), which in this embodiment is not used for communications processing.

Provided for further illustration is FIG. 4a, a detailed block diagram of the logic unit (107), as required in the alternative embodiment depicted in FIG. 3 and described above. This alternative embodiment is different in that an on-board CPU (482) is provided to perform the general processing functions that are done by the host processor (421) in the preferred embodiment. It will be self-evident to one of ordinary skill in the art that the logic unit (107) operates as a data interface in the fashion described below.

10 The PCMCIA interface (472), internal to the logic unit (107), is coupled to the controller interface (111). The PCMCIA interface (472) is also coupled to the CPU (482) and handles the communications between the processor (421) in the host computer (103) and the CPU (482). The CPU (482) is a processor capable of
15 very low standby current, such as the 16-bit Motorola 68330 processor, commercially available from Motorola, Inc., 1303 E. Algonquin Road, Schaumburg, IL.

 The PCMCIA interface (472) is mapped over a standard PCMCIA I/O port, that is configured as a standard PC COM port
20 type communication device. This PCMCIA interface is logically equivalent to the host port of a NS16550 universal asynchronous receiver/transmitter, commercially available from National Semiconductor Corporation, 2900 Semiconductor Drive, P.O. Box 58090, Santa Clara, CA, and provides the communications between
25 the host processor (421) and the on-board CPU (482). The on-board CPU (482) executes the radio control software, which is stored in ROM (484). Memory for the CPU (482) consists of factory programmable ROM (484), including memory for the storage of configuration information, and RAM (480) to store data, such as,
30 messages. The configuration information is stored, for example, in EEPROM (105) or in flash memory.

 Also included in the logic unit (107) are PCMCIA support functions (472) and power supply management (474). The power supply management (474) interfaces to the battery (315), the CPU

(482), and the host processor (421) via the controller interface (111). The power supply management block (474) provides the appropriate power supply voltage from the battery (315) and controls the application of power to the wireless packet data communication modem (101), given the various states of power on/off and sources of power between the computer (103) and wireless packet data communication modem (101).

Modem logic and radio control (478) supports communication with the RF channel, being coupled to the CPU (482) and the transceiver, i.e. modulator (417), demodulator (409), and control input (405). The modem logic and radio control (478) programs the synthesizer (404) via control input (405) and provides control for the transceiver via 420 and 422. The modem logic (478) provides functions, such as, Forward Error Correction, Block Assembly/Disassembly, Frame Sync Detection, Automatic Level Control, and Message ID Detect among others.

The logic unit (107) is preferably substantially embodied in a semi-custom designed Application Specific Integrated Circuit (ASIC). The combination of concern and care toward space conservation known in the art, standard off-the-shelf components, together with high levels of integration in a custom ASIC provides a design that can be implemented on a printed circuit board (PCB) substantially compatible with the PCMCIA Type II format or an extended version thereof. The PCB has the approximate dimensions of 46mm x 135mm.

The on-board CPU (482), in conjunction with the RAM (480), antenna (119), and its own battery (315), preferably off-the-shelf alkaline cells, enable stand-alone operation, specifically, the ability of the wireless packet data communications modem (101) to send and receive messages, even when physically disassociated from the computer (103).

It is also contemplated that the stand-alone wireless packet data communications modem may include user input/output (I/O), such as switches, pushbuttons, a touchscreen, or a display,

for example, Light Emitting Diodes (LEDs) or Liquid Crystal Display (LCD). These elements are coupled to the CPU (482) so as to cooperatively operate to provide user I/O, such as battery low indication, message waiting indication, and transceiver-in-range indication, as is known in the art.

Appreciation of a method embodiment of the preferred embodiment of the instant invention will be facilitated by a description of the FIG. 4 computing device in a first operating mode. This description refers to and describes the FIG. 5 data structure diagram in conjunction with the FIG. 7 process flow diagram.

Referring jointly to FIG. 5 and FIG. 7, representing a first operating mode of data transmission, raw data sequence (505) represents a message or data to be transmitted. The raw data sequence (505) may be provided by the user or a software application. A complete data message is constructed from the raw data sequence at step (700) by the computer (103). The data message is parsed at step (705) into individual packets (510-535). A data link header (540) is added at step (710) to each packet (510...). In a preferred embodiment, each data link header (540) and packet (510) combination is broken down into smaller six-byte transmit data blocks (545-565), which are sent at step (715) by the processor (421) to the controller interface (111). At step (720) the logic unit (107) receives the transmit data blocks (545-565) from the controller interface (111).

The logic unit (107) constructs a transmit data waveform from the transmit data blocks (545-565) at step (725). In order to create the transmit data waveform (580), error correction or parity bits (570-575) are calculated and appended to each of the transmit data blocks (545, 565). The transmit data blocks (545-565) and error correction/parity information (570-575) are then interleaved, as is well known in the art, to increase the percentage of error recovery and reduce packet re-transmission attempts. The logic unit (107) buffers the data and waits for an available channel at step (730).

When a channel is available, the logic unit (107) enables the transmitter (406) and sets the T/R switch (410) to the transmit state at step (735). The interleaved transmit data blocks (545-565) are sent to the transceiver (109) as a transmit data waveform (580). At
5 step (740) a radio frequency carrier is modulated by the transmit data waveform (580), as is known in the art.

In a preferred embodiment of the present invention, an Automatic-Repeat Request (ARQ) protocol, such as Go-Back-N ARQ is implemented. The ARQ protocol is effected at step (745) by
10 the processor (421), as is known in the art. If a packet is requested to be re-transmitted, the method as described above is repeated according to the ARQ protocol implemented.

Appreciation of an alternative method embodiment of the preferred embodiment of the instant invention may be facilitated
15 by a description of the FIG. 4 computing device in a second operating mode. This description refers to and describes the FIG. 6 data structure diagram in conjunction with the FIG. 8 process flow diagram.

Referring jointly to FIG. 6 and FIG. 8, representing a second
20 operating mode of data reception, a data modulated radio frequency carrier is received at step (800) by the receiver (402) utilizing the antenna (119). The radio frequency carrier is demodulated at step (805) and a demodulated data signal (680) is provided to the logic unit (107) at step (810).

25 The logic unit (107) de-interleaves the demodulated data signal into data blocks (645-665) and error correction is performed at step (815) using parity and error correction information (670-675). At step (817) the logic unit (107) determines the total number of data blocks in the packet by extracting the information from the
30 header data blocks (645-650), which comprise the packet's data link header (640).

The error-corrected data blocks (645-665) are sent to the controller interface (111) by the logic unit (107) at step (820). At step (825) the computer (103) receives the error-corrected data blocks

(645-665) from the controller interface (111). The computer (103) assembles the error-corrected header data blocks (645-650) into a data link header (640) and error-corrected data blocks (655-665) into a packet (610) at step (830). In a preferred embodiment, an ARQ
5 protocol is effected as part of step (830) by the computer (103) to request the re-transmission of any packet received that is not in accordance with the ARQ protocol implemented.

The computer (103) determines whether duplicate packets have been received at step (835) and discards any duplicates. This
10 could occur based on the ARQ scheme being used. At step (840) a data message is constructed from error-corrected data blocks (645-665) by re-assembling a data message (605) from the packets (610-635). The data message (505) is buffered by the computer (103) whenever required, such as when multiple messages have been
15 received.

Thus it will be appreciated by those of ordinary skill in the art that the apparatus and method disclosed provide a small, light-weight, low-cost, power-saving radio-frequency modem for use in wireless data communications. Furthermore, the present
20 invention satisfies the long-felt need of mobile data computing by providing two-way wireless communications for the general-purpose computing device. In addition, the present invention enables the user to receive and send data even when the wireless packet data communications modem is physically disassociated
25 from the host computer.

It will be apparent to those skilled in the art that the disclosed invention may be modified in numerous ways and may assume many embodiments other than the preferred form specifically set out and described above.

30 Accordingly, it is intended by the appended claims to cover all modifications of the invention which fall within the true spirit and scope of the invention.

What is claimed is:

Claims

1. A wireless packet data communications modem,
comprising:
 - 5 a transceiver having a control input, a modulator for impressing modulation on a radio frequency carrier, and a demodulator for providing a demodulated data signal, and
 - a logic unit, coupled to said modulator, said demodulator, said control input, and a controller interface, for
 - 10 providing, in response to a transmit data block at said controller interface, a data wave form input to said modulator and for providing, responsive to said demodulated data signal, error corrected data blocks to said controller interface.

2. The wireless packet data communications modem of claim 1, wherein said controller interface substantially complies to the Personal computer memory card international association electrical standard.
- 5 3. The wireless packet data communications modem of claim 2, further comprising:
a housing for containment of said modem, said housing conforming substantially to the Personal computer memory card international association Type II format.
- 10 4. The wireless packet data communications modem of claim 2, further comprising:
a housing for containment of said modem, said housing conforming at least in part to the Personal computer memory card international association Type II format.
- 15 5. The wireless packet data communications modem of claim 1, wherein said transceiver is configured to operate as a frequency division multiple access transceiver.
- 20 6. The wireless packet data communications modem of claim 1, wherein said transceiver is configured to operate as a time division multiple access transceiver.
- 25 7. The wireless packet data communications modem of claim 1, wherein said transceiver is configured to operate as a code division multiple access transceiver.
- 30 8. The wireless packet data communications modem of claim 1, wherein said transceiver is configured to operate as a frequency hopped spread spectrum transceiver.

9. The wireless packet data communications modem of claim 1, wherein said modulation is frequency shift keyed modulation.
10. The wireless packet data communications modem of claim 5 9, wherein said frequency shift keyed modulation is a four level modulation.
11. The wireless packet data communications modem of claim 9, wherein said modulation is two level modulation.
- 10 12. The wireless packet data communications modem of claim 1, wherein said modulation is a linear form of modulation.
13. The wireless packet data communications modem of claim 15 1, wherein said error-corrected data blocks have been de-interleaved, error corrected, and buffered prior to providing said error corrected blocks to said controller interface.

14. A computing device with wireless packet data communications capability, comprising:
- a transceiver having a control input, a modulator for impressing modulation on a radio frequency carrier, and a demodulator for providing a demodulated data signal,
 - 5 a logic unit, coupled to said modulator, said demodulator, said control input, and a controller interface, for providing, responsive to control information at said controller interface, transceiver control information at said control input, said logic
 - 10 unit further providing, in response to a transmit data block at said controller interface, a data wave form input to said modulator, and for providing, responsive to said demodulated data signal, an error corrected data block to said controller interface, and
 - 15 a computer, coupled to said controller interface, and having a memory, a processor, a power source, and an operator interface, said computer providing said control information and said transmit data block to said controller interface and receiving said error corrected data blocks.

15. The computing device recited in claim 14, wherein said computer providing said transmit data block includes parsing a raw data sequence into a plurality of said transmit data blocks.
- 5 16. The computing device recited in claim 15, wherein said raw data sequence is provided by an application.
17. The computing device recited in claim 15, wherein said control information includes an operating parameter for said
10 transceiver.
- 18 The computing device recited in claim 14, further including a first housing for containment of said computer and a second housing for containment of said transceiver and said logic unit,
15 said second housing disposed in part within said first housing.
19. The computing device recited in claim 18, wherein said second housing conforms substantially to PCMCIA standards.
- 20 20. The computing device recited in claim 18, said second housing being removable from said first housing.
21. The computing device recited in claim 20, further comprising:
25 a separate power source for providing power to said transceiver and said logic unit.
22. The computing device recited in claim 21, further comprising:
30 an antenna mechanically coupled to said second housing and electrically coupled to said transceiver.
23. The computing device of claim 14, wherein said controller interface substantially complies to the PCMCIA electrical standard.

24. The computing device of claim 14, wherein said modulation is frequency shift keyed modulation.

5 25. The computing device of claim 24, wherein said frequency shift keyed modulation is a 4 level modulation.

26. The computing device of claim 24, wherein said frequency shift keyed modulation is a 2 level modulation.

10

27. The computing device of claim 14, wherein said error-corrected data block has been de-interleaved, error corrected, and buffered prior to providing said error corrected block to said controller interface.

28. In a computing device having wireless packet data communications capability, said computing device including a packet data transceiver, a logic unit, and a computer, a method including the steps of:

- 5 receiving a radio frequency carrier having data modulation, providing a demodulated data signal to said logic unit, providing, responsive to said demodulated data signal, error corrected data blocks to a controller interface,
- 10 receiving at said computer, said error corrected data blocks at said controller interface,
- constructing, responsive to said data blocks, a data message.

29. The method recited in claim 28, further comprising the step of effecting any ARQ protocol.

30. The method recited in claim 29, further comprising the step
5 of determining whether any of said error corrected data blocks are duplicate data blocks.

31. The method recited in claim 30 further comprising the step
10 of buffering at said computer a plurality of said data messages.

32. In a computing device having wireless packet data communications capability, said computing device including a packet data transceiver, a logic unit, and a computer, a method including the steps of:

- 5 constructing a complete packet data message from raw data,
 parsing said data message into data blocks,
 adding header information to said data blocks,
 transmitting by said computer said header information with
 said data blocks to a controller interface,
- 10 receiving said header information and said data blocks from
 said controller interface at said logic unit,
 constructing, responsive to said header information and
 said data blocks, a transmit data wave form,
 enabling said transceiver to transmit, and
- 15 modulating, responsive to said transmit data wave form, a
 radio frequency carrier provided by said transceiver.

33. The method recited in claim 32, further comprising the step of effecting any ARQ protocol.

34. The method recited in claim 33, further comprising the step
5 of waiting for an available radio frequency channel.

35. A wireless packet data communications modem, comprising:

a transceiver having a control input, a modulator for impressing modulation on a radio frequency carrier, and a

5 demodulator for providing a demodulated data signal,

a logic unit, coupled to said modulator, said demodulator, said control input, and a controller interface, said logic unit operating as a data interface between said controller interface and said transceiver, and

10 a housing for containment of said wireless packet data communications modem, said housing conforming at least in part to the Personal computer memory card international association Type II standard.

36. The wireless packet data communications modem of claim 35, wherein said controller interface substantially complies to the Personal computer memory card international association electrical standard.
- 5 37. The wireless packet data communications modem of claim 36, wherein said housing conforms substantially to the Personal computer memory card international association Type II standard.
- 10 38. The wireless packet data communications modem of claim 35, wherein said transceiver is configured to operate as a frequency division multiple access transceiver.
- 15 39. The wireless packet data communications modem of claim 35, wherein said transceiver is configured to operate as a time division multiple access transceiver.
- 20 40. The wireless packet data communications modem of claim 35, wherein said transceiver is configured to operate as a code division multiple access transceiver.
- 25 41. The wireless packet data communications modem of claim 35, wherein said transceiver is configured to operate as a frequency hopped spread spectrum transceiver.
42. The wireless packet data communications modem of claim 35, wherein said modulation is frequency shift keyed modulation.
- 30 43. The wireless packet data communications modem of claim 42, wherein said frequency shift keyed modulation is a four level modulation.
44. The wireless packet data communications modem of claim 42, wherein said modulation is two level modulation.

45. The wireless packet data communications modem of claim 35, wherein said modulation is a linear form of modulation.

46. A wireless packet data communications modem arranged and constructed to cooperatively operate with a computer to provide wireless data communications, the modem comprising:
- 5 a transceiver having a control input, a modulator for impressing modulation on a radio frequency carrier, and a demodulator for providing a demodulated data signal,
 - a logic unit, coupled to said modulator, said demodulator, said control input, and a controller interface, said logic unit operating as a data interface between said controller
 - 10 interface and said transceiver, and
 - a housing for containment of said modem, said housing conforming at least in part to the Personal computer memory card international association Type II standard.

47. The wireless packet data communications modem of claim 46, wherein said transceiver and said logic unit receive and transmit data when physically disassociated from said computer.

48. A computing device with wireless packet data communications capability, comprising:
- a transceiver having a control input, a modulator for impressing modulation on a radio frequency carrier, and a demodulator for providing a demodulated data signal,
 - a logic unit, coupled to said modulator, said demodulator, said control input, and a controller interface, said logic unit operating as a data interface between said controller interface and said transceiver,
 - a computer, coupled to said controller interface, and having a memory, a processor, a power source, and an operator interface, and
 - a first housing for containment of said computer and a second housing for containment of said transceiver and said logic unit, said second housing disposed in part within said first housing, said second housing conforming substantially to PCMCIA standards.

49. The computing device recited in claim 48, said second housing being removable from said first housing.

50. The computing device recited in claim 49, further
5 comprising:
a separate power source for providing power to said transceiver and said logic unit.

51. The computing device recited in claim 50, further
10 comprising:
an antenna mechanically coupled to said second housing and electrically coupled to said transceiver.

52. The computing device of claim 48, wherein said controller
15 interface substantially complies to the PCMCIA electrical standard.

53. The wireless packet data communications modem of claim 48, wherein said transceiver is configured to operate as a frequency division multiple access transceiver.
20

54. The wireless packet data communications modem of claim 48, wherein said transceiver is configured to operate as a time division multiple access transceiver.

25 55. The wireless packet data communications modem of claim 48, wherein said transceiver is configured to operate as a code division multiple access transceiver.

56. The wireless packet data communications modem of claim
30 48, wherein said transceiver is configured to operate as a frequency hopped spread spectrum transceiver.

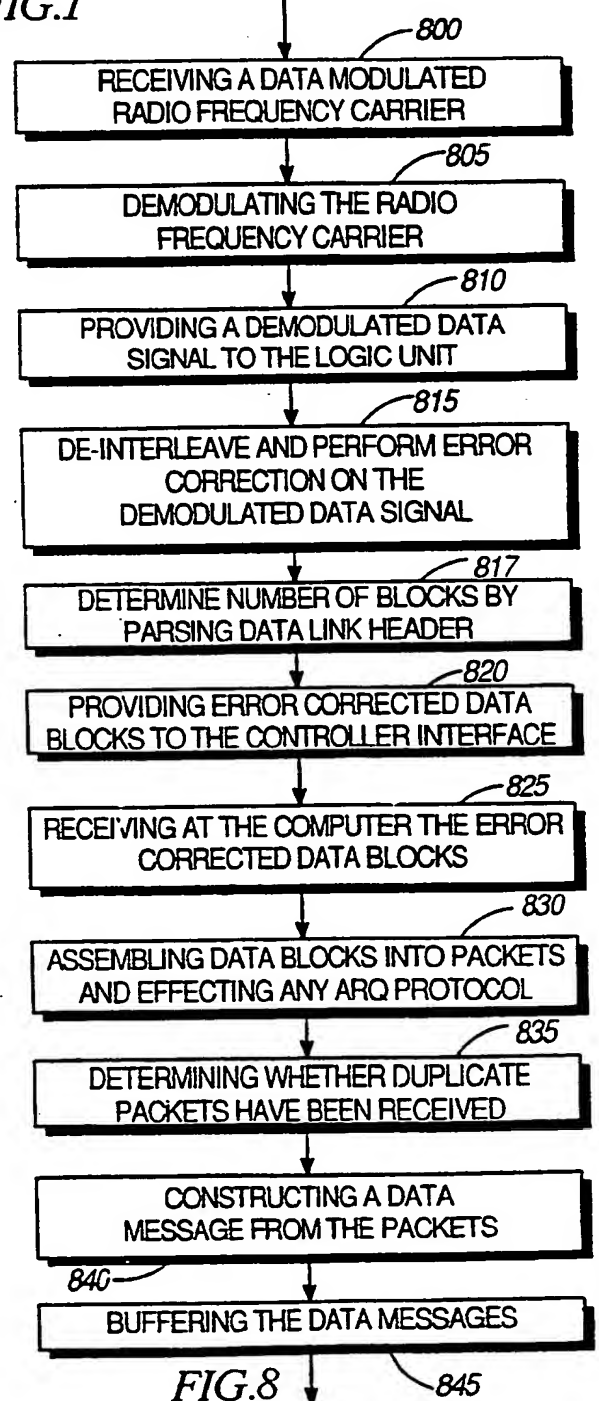
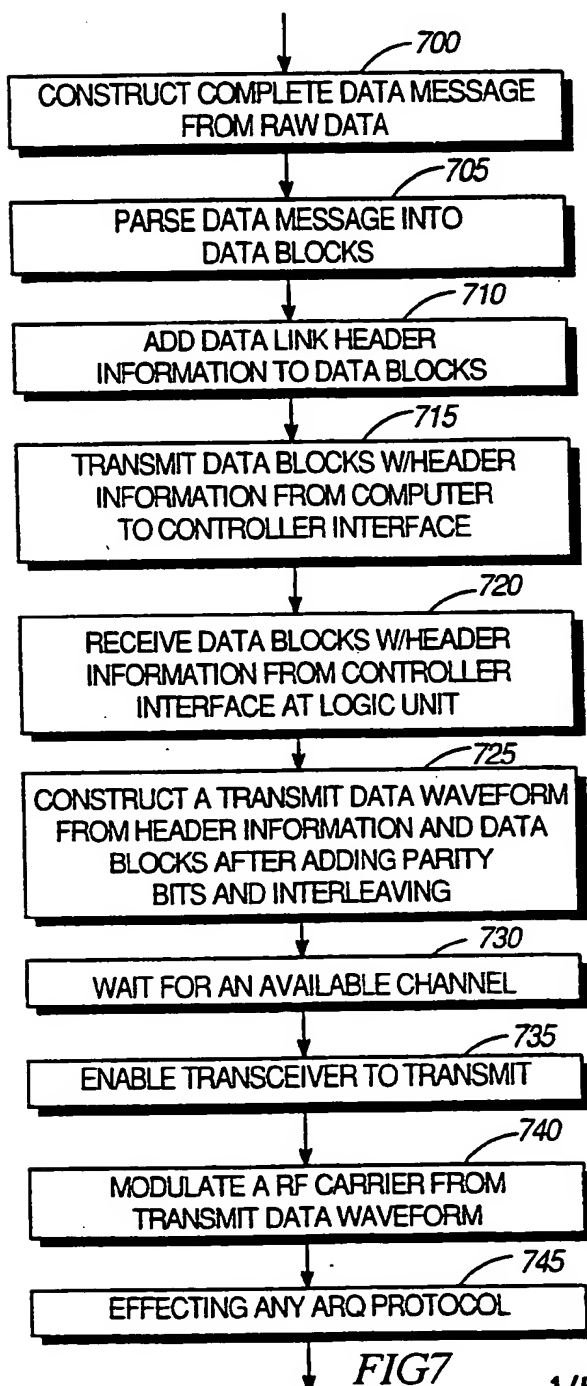
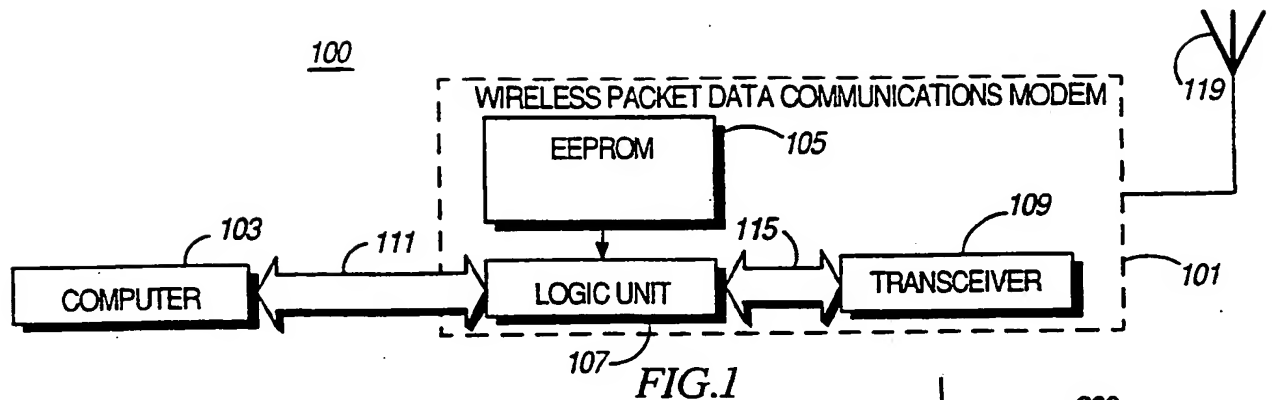
57. The computing device of claim 48, wherein said modulation is frequency shift keyed modulation.

58. The computing device of claim 57, wherein said frequency shift keyed modulation is a 4 level modulation.

59. The computing device of claim 57, wherein said frequency
5 shift keyed modulation is a 2 level modulation.

60. The computing device recited in claim 51, wherein said transceiver and said logic unit receive and transmit data when
physically disassociated from said computer.

10



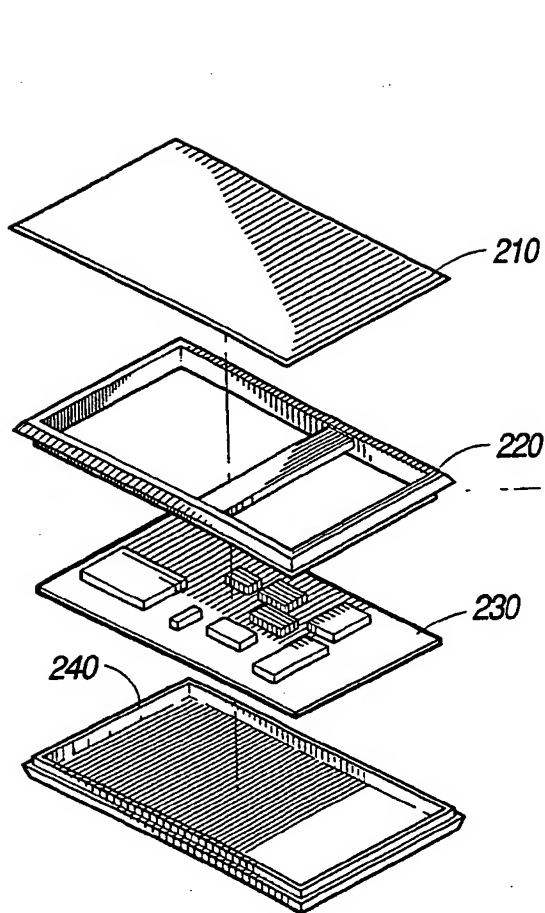


FIG. 2

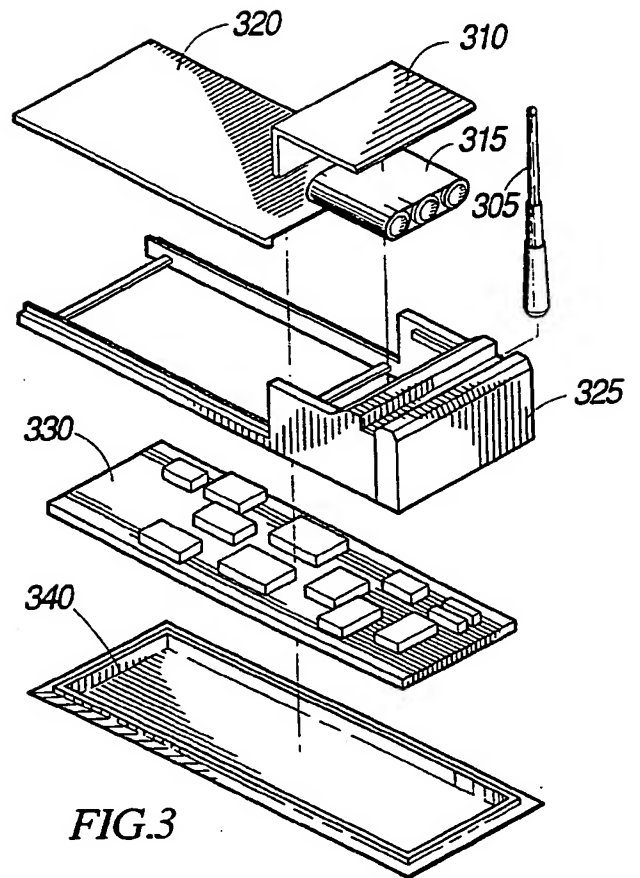


FIG. 3

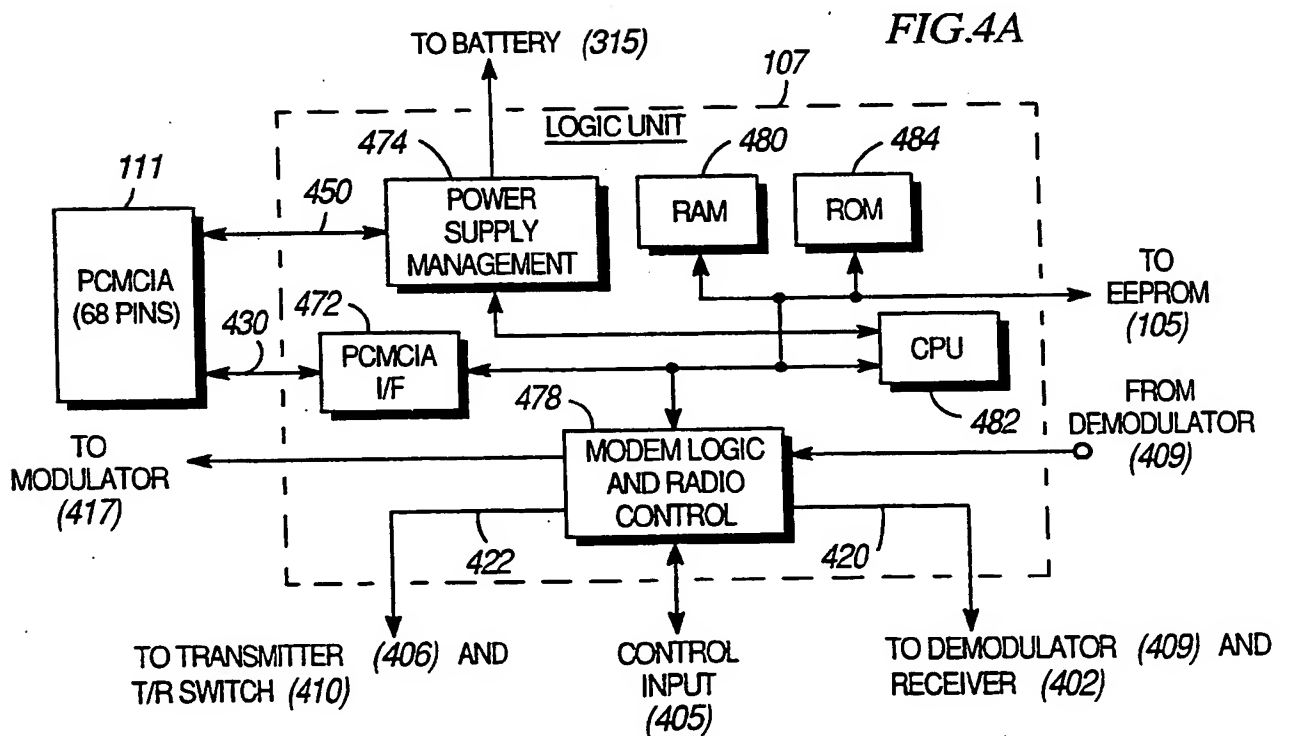


FIG. 4A

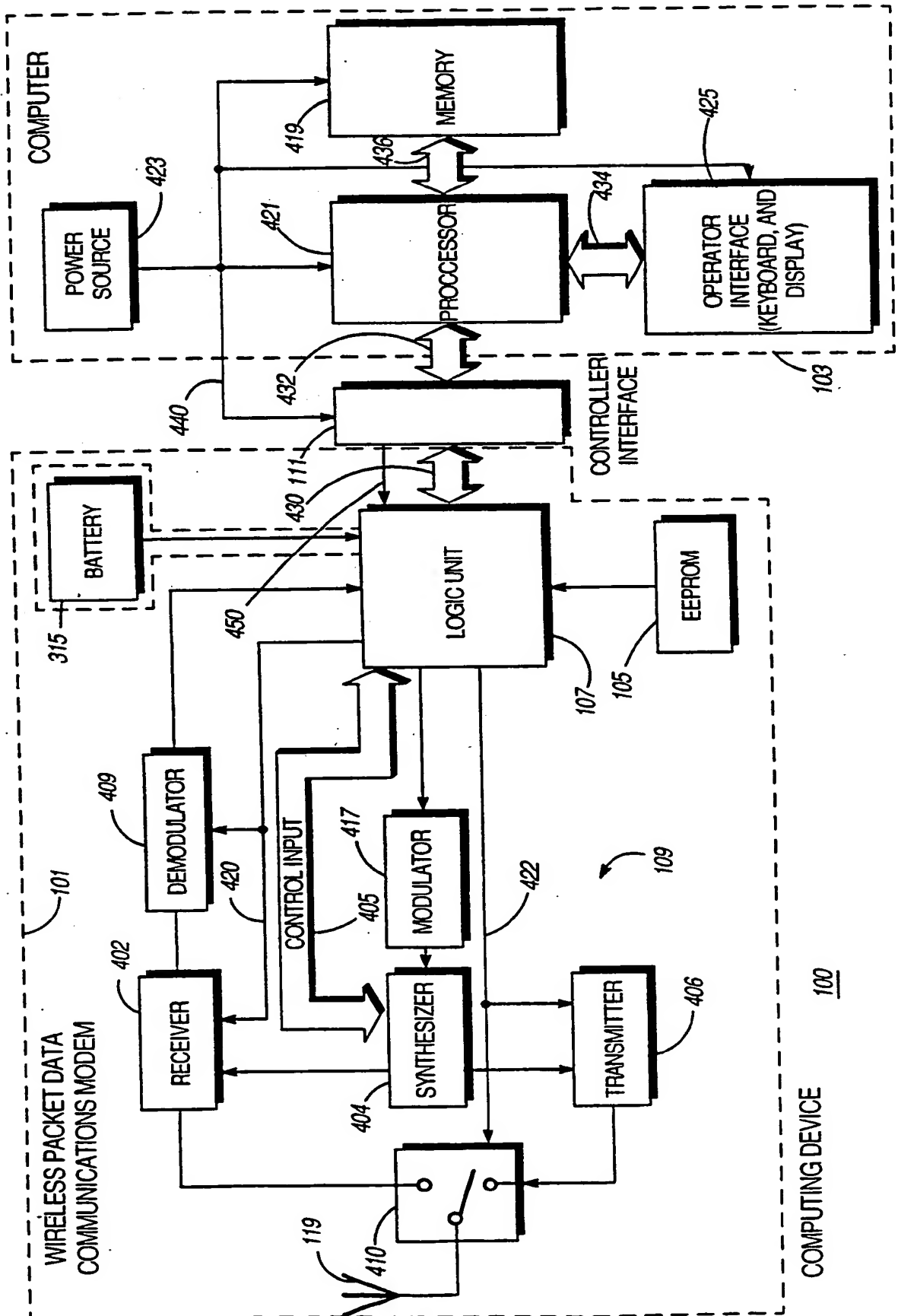


FIG.4

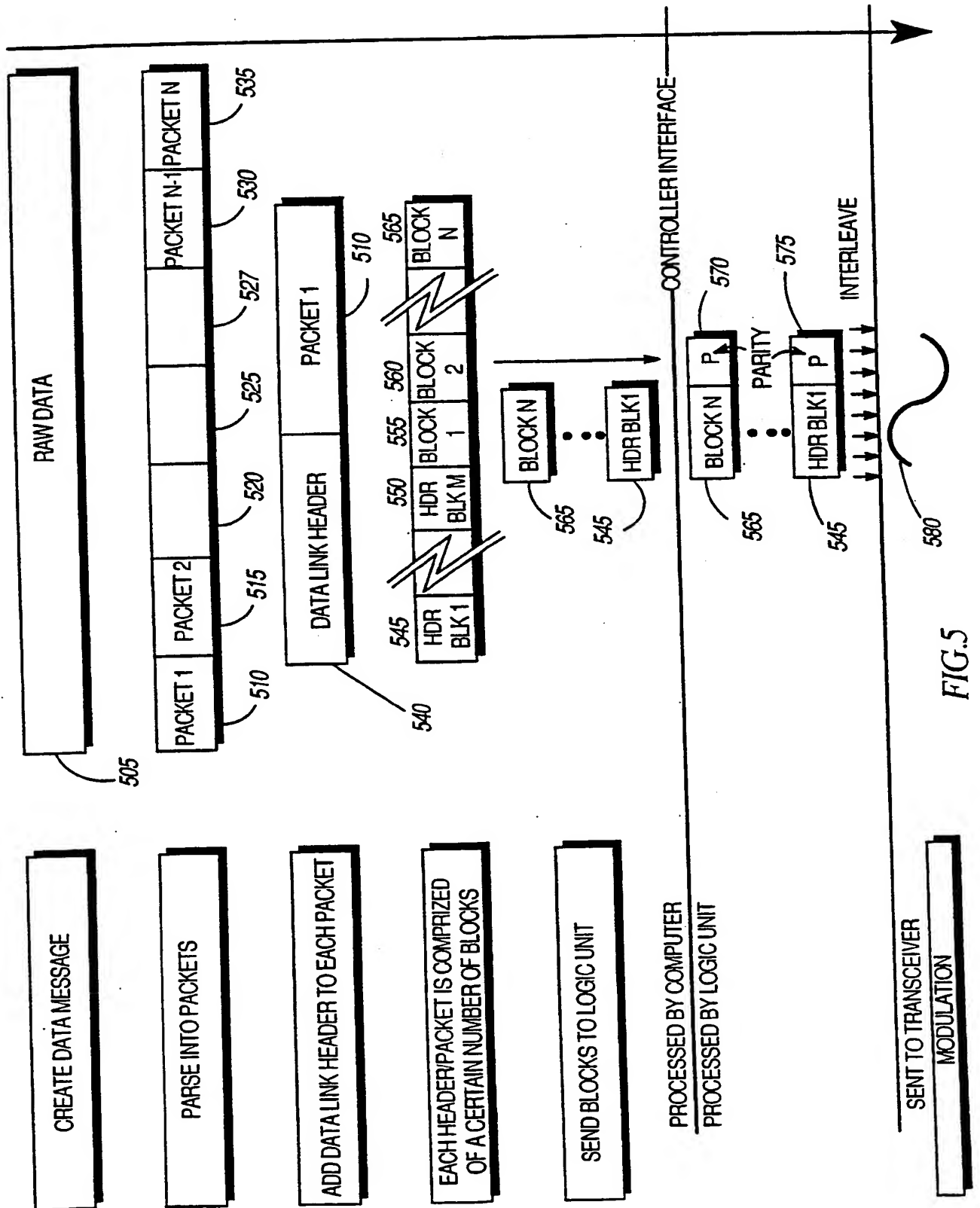
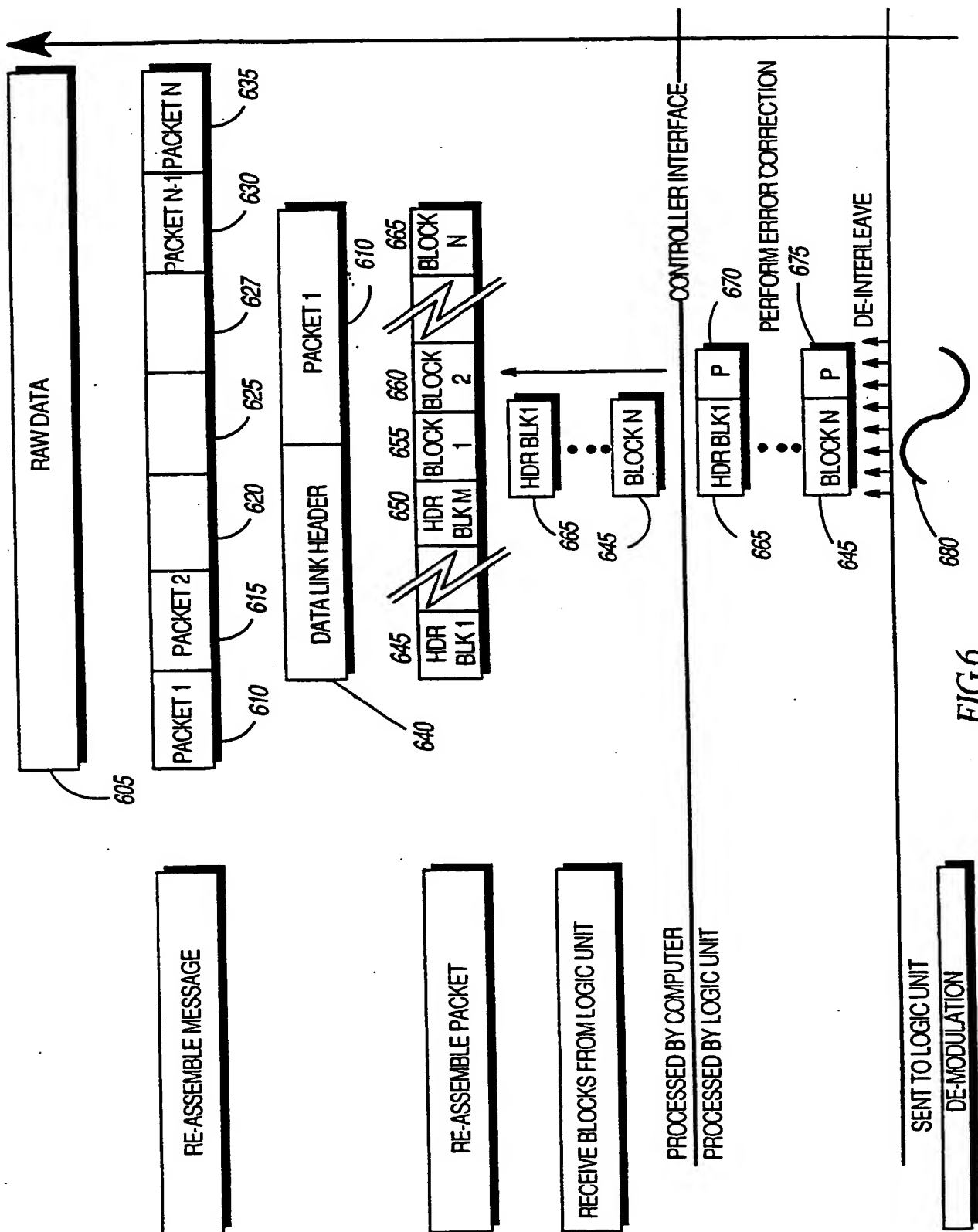


FIG. 5



INTERNATIONAL SEARCH REPORT

International application No.
PCT/US94/10323

A. CLASSIFICATION OF SUBJECT MATTER

IPC(5) :H04B 1/38; H04L 5/16, 1/00; H04J 3/00

US CL :375/7, 8; 371/30; 370/99; 455/84, 88

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 375/7, 8, 36; 371/30; 370/99; 455/73, 84, 88, 89, 90; 340/310A, 310R; 361/683, 685, 686, 725, 752

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

USPTO APS: control interfacer and logic unit, transceiver and error corrector(1a)code#, modem or (modulator and demodulator) and housing

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US, A, 4,354,252 (LAMB ET AL) 12 October 1982, see figures 1, 2A and 3, and columns 2 and 6.	1,5-11,13-17, 22, 24-29,32-44,46-48,51 and 53-59
Y	US, A, 4,972,432 (WILSON ET AL) 20 November 1990, see figures 1, 7 and 12.	1,5-11,14, 22,24-26, 28,32,35-44,46-48 and 51-59
Y	US, A, 5,050,041 (SHAFI) 17 September 1991, see figures 1-3 and columns 1, lines 15-50.	2 - 4, 18 - 21, 23,35,46 and 48-50

☒ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* "A"	Special categories of cited documents: document defining the general state of the art which is not considered to be part of particular relevance	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"E"	earlier document published on or after the international filing date	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"O"	document referring to an oral disclosure, use, exhibition or other means	"&"	document member of the same patent family
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search

04 DECEMBER 1994

Date of mailing of the international search report

JAN 19 1995

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US94/10323

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US, A, 5,201,067 (GRUBE ET AL) 06 April 1993, see figures 1-3.	1,14,28,32, 46-48 and 60
A	US, A, 4,951,309 (GROSS ET AL) 21 August 1990, see figure 1.	1,14,28,32,35,46 and 48
A	US, A, 5,033,111 (MARUI) 16 July 1991, see figure 1.	1,14,28,32, 35,46 and 48
A	US, A, 5,161,169 (GALANO ET AL) 03 November 1992, see figures 1-3	2-4,18-20, 46 and 48

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US94/10323

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This international report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:
2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

Please See Extra Sheet.

1. ☒ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐
☒

The additional search fees were accompanied by the applicant's protest.

No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US94/10323

BOX II. OBSERVATIONS WHERE UNITY OF INVENTION WAS LACKING

This ISA found multiple inventions as follows:

Group I. Claims 1-31 and 35-60, drawn to a transceiver having a modulator, demodulator, logic unit and controller interface for transmitting and receiving a data signal classified in class 375 subclass 7.

Group II claims 32-34 drawn to a transceiver comprising steps for packet formatting, transmitting and receiving a corresponding formatted packet classified in class 370 subclass 99.

Noting in particular that the method and means for transmitting and receiving in group I does not include the step for packet formatting claimed in group II.

Since the claims of different groups, groups I-II, do not share or have in common the same special technical feature, packet formatting, as indicated above, there is no unity between the groups.

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